Problem 1 (4+1 points)

a) Draw the logic circuit corresponding to the following logic expression. Use only 2-input AND gates, 2-input OR gates, 2-input XOR gate and 1-input NOT gate.

b) Determine output Y when inputs A='1', B='0' and C='1'.

c) \( Y = ((\neg (\neg (A \land B)) \lor \neg C) \oplus A) \land (A \lor \neg C) \)

Solution a)

![Logic Circuit Diagram]

d) Solution b) \( Y = '0' \).

Problem 2 (1.5 +1.5 points)

a) Implement NOT function using XOR logic gate.

b) Similarly, implement NOT function using XNOR logic gate.

Solution a) and b)
Problem 3 (3.5+1.5 points)

a) Write the Truth –table for the following logic expression.

\[ Y = \text{NOT}((A \text{ AND } B) \text{ OR}(B \text{ AND } C) \text{ OR } (C \text{ AND } A)) \text{ XOR } \text{NOT}(A) \]

b) Based on the truth table, draw the two-level logic diagram. You can use three-input gates.

Solution a)

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<th></th>
<th>A</th>
<th>B</th>
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Solution b)

![Logic Diagram](image)

(If you have used XOR gate, its fine.)

Problem 4 (3.5 +1.5 points)

a) Complete a truth table for the transistor-level circuit given below.
b) Complete a truth table for the transistor-level circuit given below. Replace the circuit with a logic gate.

\[
\begin{array}{cccc}
\text{A} & \text{B} & \text{C} & \text{OUT} \\
0 & 0 & 0 & 1 \\
0 & 0 & 1 & 1 \\
0 & 1 & 0 & 1 \\
0 & 1 & 1 & 0 \\
1 & 0 & 0 & 0 \\
1 & 0 & 1 & 0 \\
1 & 1 & 0 & 0 \\
1 & 1 & 1 & 0 \\
\end{array}
\]

Logic gate:

Problem 5 (3.5+1.5 points)
a) Use 2:1 Multiplexers to implement an 8:1 multiplexer. (Hint: We use three 2:1 multiplexers to implement a 4:1 multiplexer)

b) In your diagram, label inputs i0 – i7, and use select line 5_{10} to determine output Y.

Solution a) and b)

![Diagram](image1)

Problem 6 (2 points)

Complete the table below. A, B and C_{in} are the inputs to a full adder. S is the sum bit, and C_{out} is the carry-out bit.

<table>
<thead>
<tr>
<th>A</th>
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<th>C_{in}</th>
<th>S</th>
<th>C_{out}</th>
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