ECE/CS 252 Fall 2011 Homework 3 (25 points)
Due in Discussion Wednesday, October 05, 2011

Instructions: You should do this homework in the groups assigned to you in discussion. You should hand in ONE copy of the homework that lists your discussion section number and names and UW ID numbers of all students. You must *staple* all pages of your homework together to receive full credit.

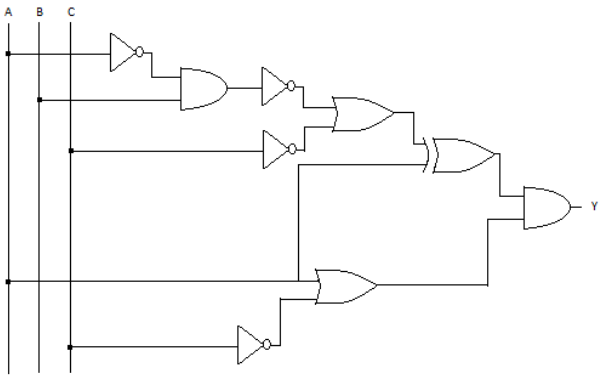
Warning: Most homework will use questions from your textbook, Patt and Patel's *Introduction to Computing Systems*, which we abbreviate (*ItCS*) .

First contact for questions is TA Preeti Agarwal: pagarwal7@wisc.edu

Problem 1 (4+1 points)

a) Draw the logic circuit corresponding to the following logic expression. Use only 2- input AND gates, 2- input OR gates, 2-input XOR gate and 1- input NOT gate.
b) Determine output Y when inputs A='1', B='0' and C='1'.
c) Y= (((NOT(NOT(A) AND B)) OR NOT(C))XOR A) AND (A OR NOT (C))

Solution a)



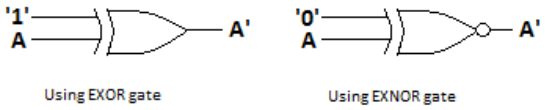
d) **Solution b)** Y= '0'.

Problem 2 (1.5 +1.5 points)

a)Implement NOT function using XOR logic gate.

b) Similarly, implement NOT function using XNOR logic gate.

Solution a) and b)



Using EXOR gate Using EXNOR gate

Problem 3 (3.5+1.5 points)

a)Write the Truth –table for the following logic expression.

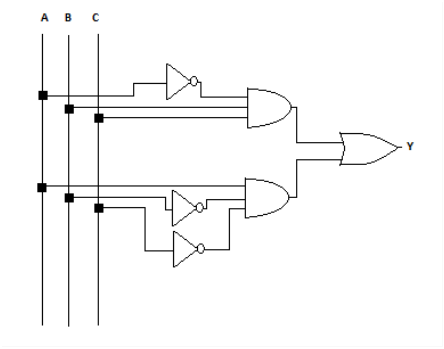
Y= (NOT((A AND B) OR(B AND C) OR (C AND A))) XOR (NOT(A))

b) Based on the truth table, draw the two-level logic diagram. You can use three- input gates.

Solution a)

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

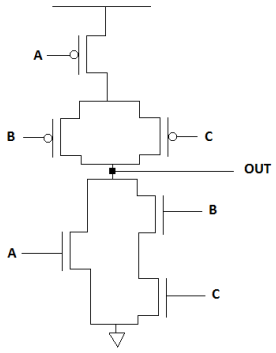
Solution b)



(If you have used XOR gate, its fine.)

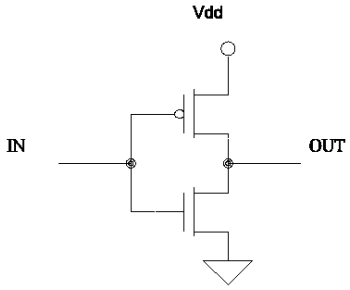
Problem 4 (3.5 +1.5 points)

a) Complete a truth table for the transistor-level circuit given below.



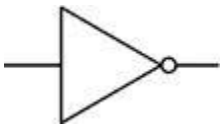
A	B	C	OUT
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

b) Complete a truth table for the transistor-level circuit given below. Replace the circuit with a logic gate.



IN	**OUT**
0	**1**
1	**0**

Logic gate:

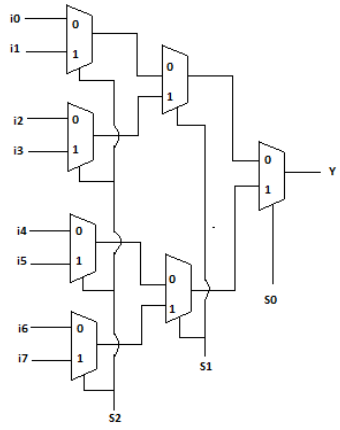


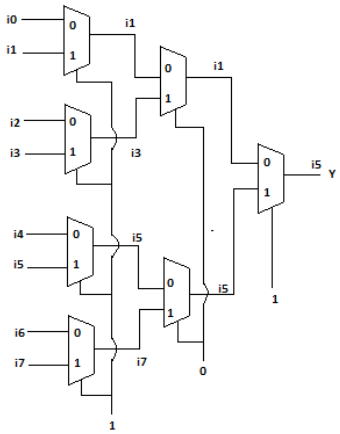
Problem 5 (3.5+1.5 points)

a) Use 2:1 Multiplexers to implement an 8:1 multiplexer. (Hint: We use three 2:1 multiplexers to implement a 4:1 multiplexer)

b) In your diagram, label inputs i0 – i7, and use select line 5_{10} to determine output Y.

Solution a) and b)





Problem 6 (2 points)

Complete the table below. A, B and C_{in} are the inputs to a full adder. S is the sum bit, and C_{out} is the carry-out bit.

A	B	C_i	S	C_{i+1}
0	**0**	**0**	0	0
0	**0**	1	1	0
1	1	0	**0**	**1**
1	**1**	**1**	1	1