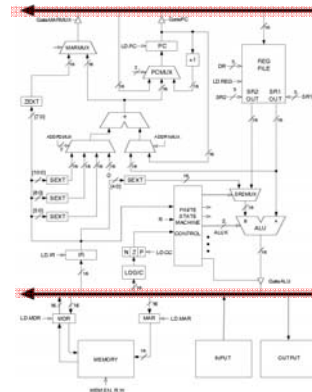# LC-3 Datapath

ECE/CS 252, Fall 2010
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LC-3 Data Path Revisited

Filled arrow
= info to be processed.
**Unfilled arrow**
= control signal.

Data Path Components

Global bus

- special set of wires that carry a 16-bit signal to many components
- inputs to the bus are "tri-state devices," that only place a signal on the bus when they are enabled
- only one (16-bit) signal should be enabled at any time
  - ➤ control unit decides which signal "drives" the bus
- any number of components can read the bus
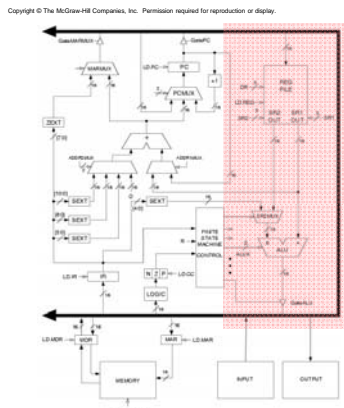 - ➤ register only captures bus data if it is write-enabled by the control unit

Output

Enable
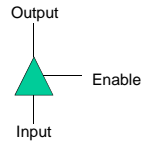
Input

Memory Access
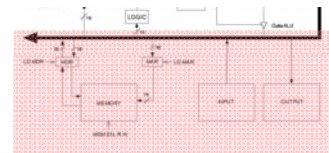
Control and data registers for memory and I/O devices
Memory: MAR, MDR (also control signal for read/write)

Register File and ALU

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Data Path Components

ALU

- Accepts inputs from register file and from sign-extended bits from IR (immediate field).
- Output goes to bus.
  - ➤ used by condition code logic, register file, memory

Register File

- Two read addresses (SR1, SR2), one write address (DR)
- Input from bus
  - ➤ result of ALU operation or memory read
- Two 16-bit outputs
  - ➤ used by ALU, PC, memory address
  - ➤ data for store instructions passes through ALU

Fetch and Memory Address Generation
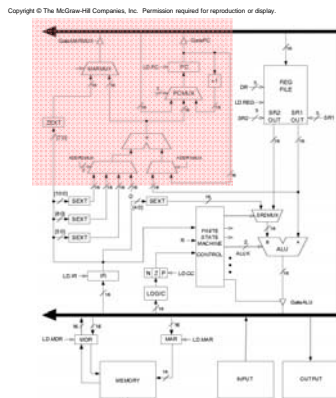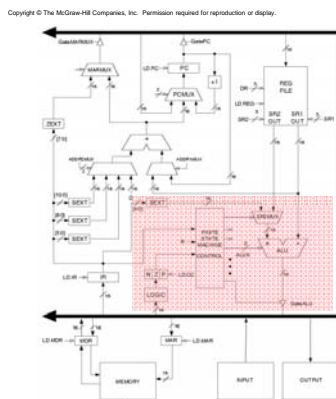
Data Path Components

PC and PCMUX

- **Three inputs to PC, controlled by PCMUX**
  1. **PC+1 – FETCH stage**
  2. **Address adder – BR, JMP**
  3. **bus – TRAP (discussed later)**

MAR and MARMUX

- **Two inputs to MAR, controlled by MARMUX**
  1. **Address adder – LD/ST, LDR/STR**
  2. **Zero-extended IR[7:0] -- TRAP (discussed later)**

Condition Code Logic and Control Unit

Data Path Components

Condition Code Logic

- **Looks at value on bus and generates N, Z, P signals**
- **Registers set only when control unit enables them (LD.CC)**
  - ➤ **only certain instructions set the codes**
    (ADD, AND, NOT, LD, LDI, LDR, LEA)

Control Unit – Finite State Machine

- **On each machine cycle, changes control signals for next phase of instruction processing**
  - ➤ **who drives the bus?** (GatePC, GateALU, …)
  - ➤ **which registers are write enabled?** (LD.IR, LD.REG, …)
  - ➤ **which operation should ALU perform?** (ALUK)
  - ➤ **…**
- **Logic includes decoder for opcode, etc.**

Summary

LC-3 Data Path

- **Global Bus**
- **Memory Interface**
- **Register File and ALU**
- **Fetch and Memory Address Generation**
- **Condition Code Logic**
- **Control Unit**

Just one way to build the data path for this ISA

Alternatives may:

- **Consume less power**
- **Provide better performance, clock frequency**