

CS/ECE 252: INTRODUCTION TO COMPUTER ENGINEERING

UNIVERSITY OF WISCONSIN – MADISON

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Midterm Examination 2

In Class (50 minutes)

Wednesday, October 29, 2008

Weight: 15%

NAME:

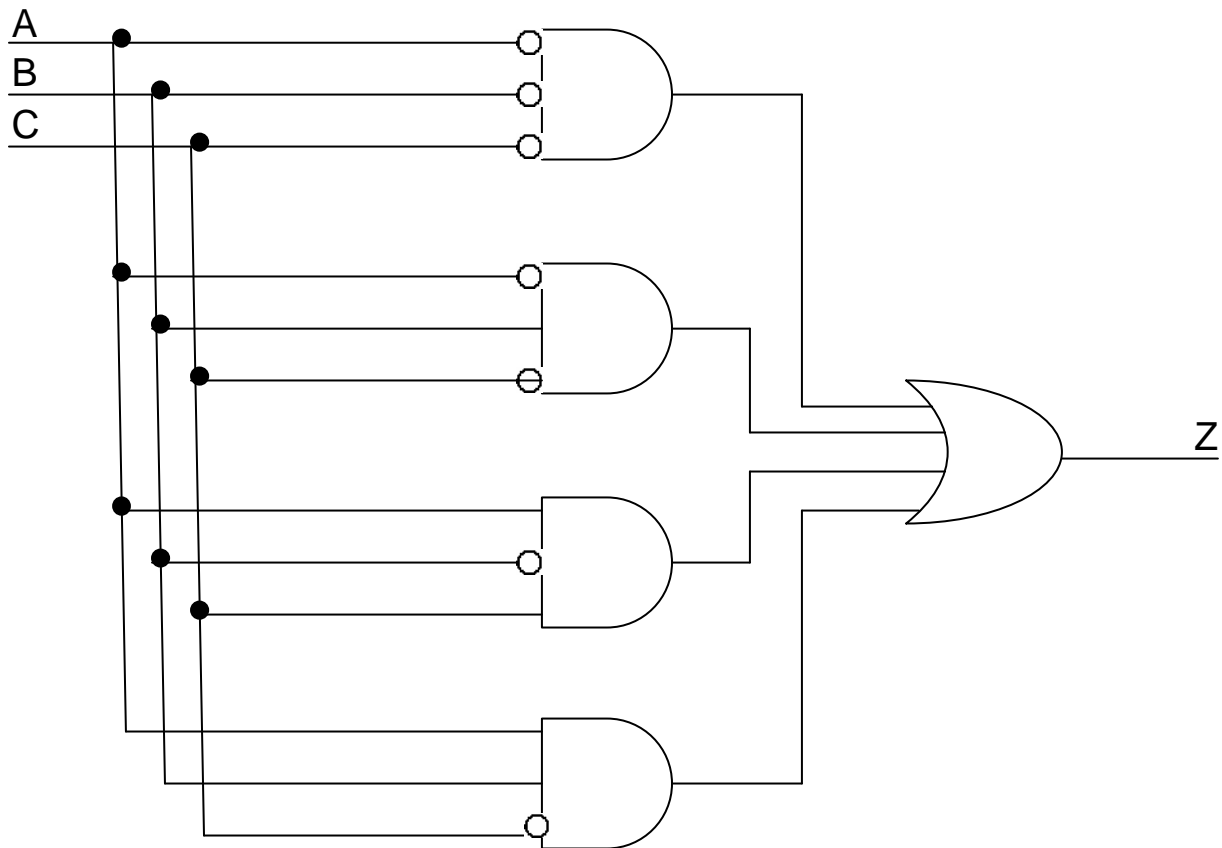
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**Please show your work in order to receive partial credits.
You may only have pencil and eraser on the desk, everything else is on the floor.
Also, please turn off your cell phone, -5 points for a cell phone ring!!!!!!
You should have a total of 8 pages, please check accordingly.**

Problem 1 (8 points)

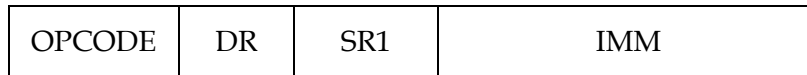
Draw the decoder based implementation of the truth table below.

Inputs			Output
A	B	C	Z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0



Problem 2 (9 points)

Suppose a 32-bit instruction takes the following format:



If there are 122 opcodes and 250 registers:

- a) What is the minimum number of bits required to represent the OPCODE?

Answer: 7 bits

- b) What is the minimum number of bits required to represent the destination register DR AND source register SR1? (Give the total number of bits.)

Answer: 16 bits

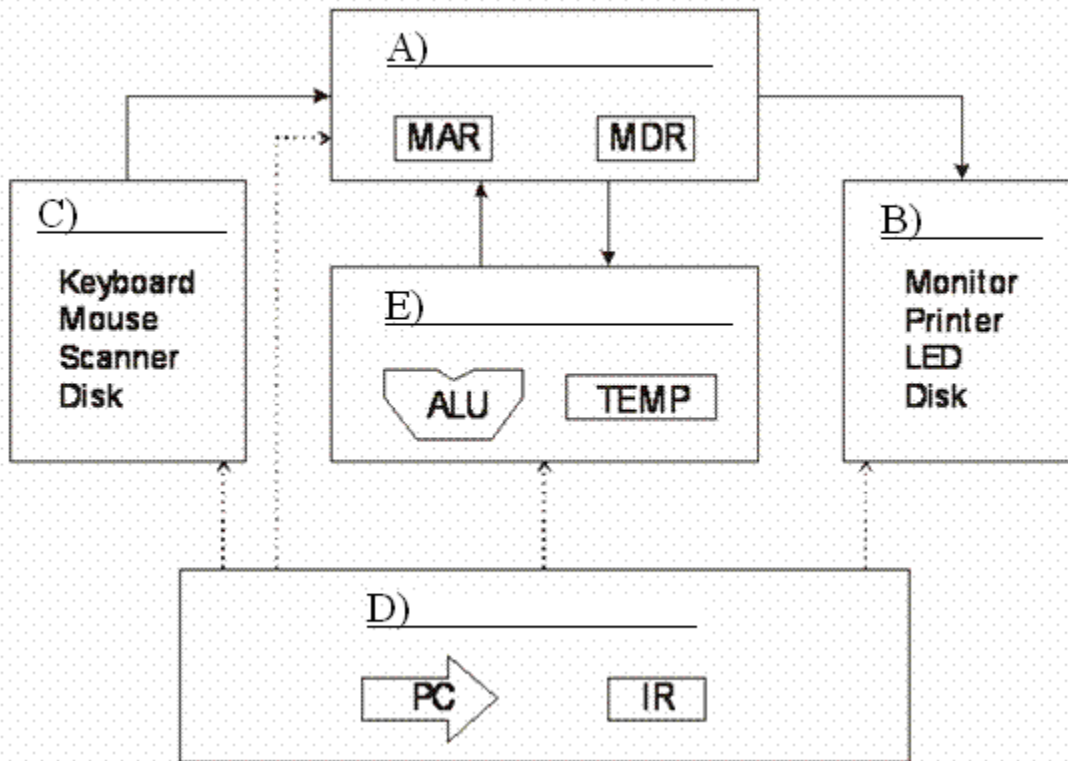
- c) Assuming the IMM (immediate) represents a 2's complement value, what is the range (lower and upper bounds) of signed numbers that an IMM type instruction can use?

Answer: 9 bits remain

Range: -256 to 255

Problem 3 (10 points)

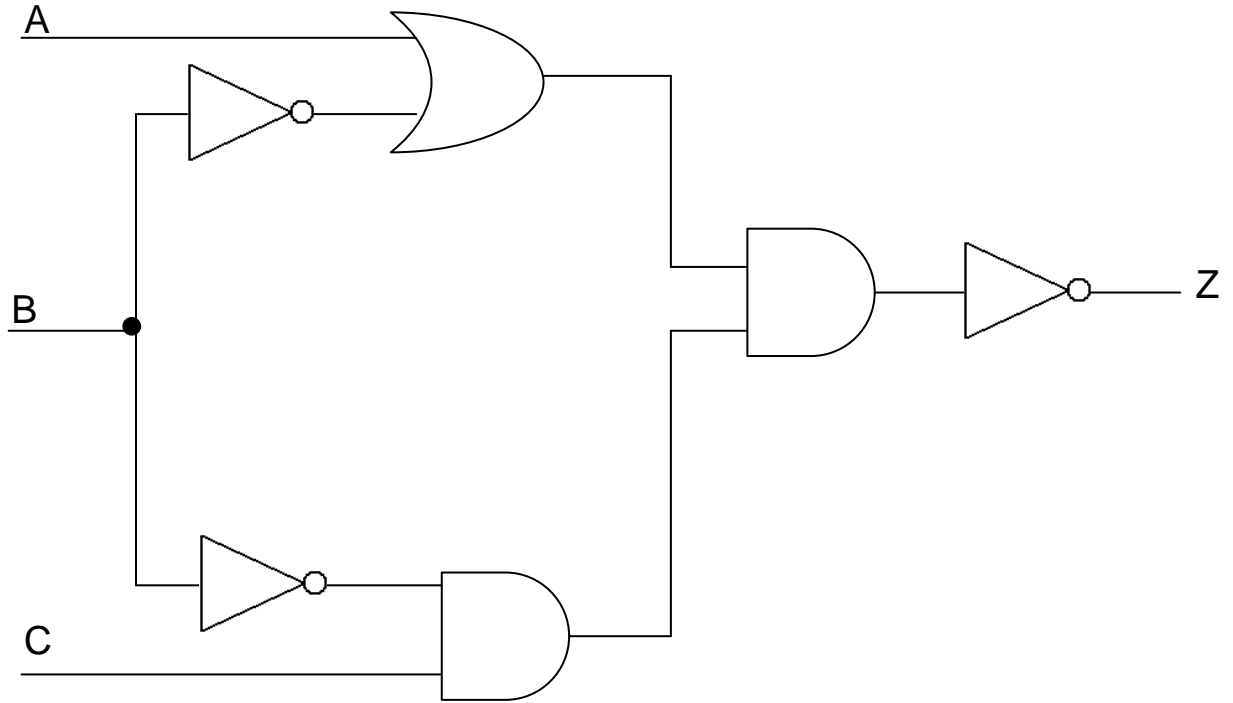
Below is the block diagram for the von Neumann model without the names of its five components. In the spaces below, write the name and briefly describe each of the parts of the von Neumann model.



- A) Memory: An addressable space which is used for storing information in the computer.
- B) Output: The devices that allow us to receive the output of the work processed by the computer.
- C) Input: The devices that allow us to give information to the computer for processing.
- D) Control Unit: Tracks where we are within the process of executing a program and where we are in the process of executing an instruction.
- E) Processing Unit: Place where the actual processing of information is carried out in the computer.

Problem 4 (8 points)

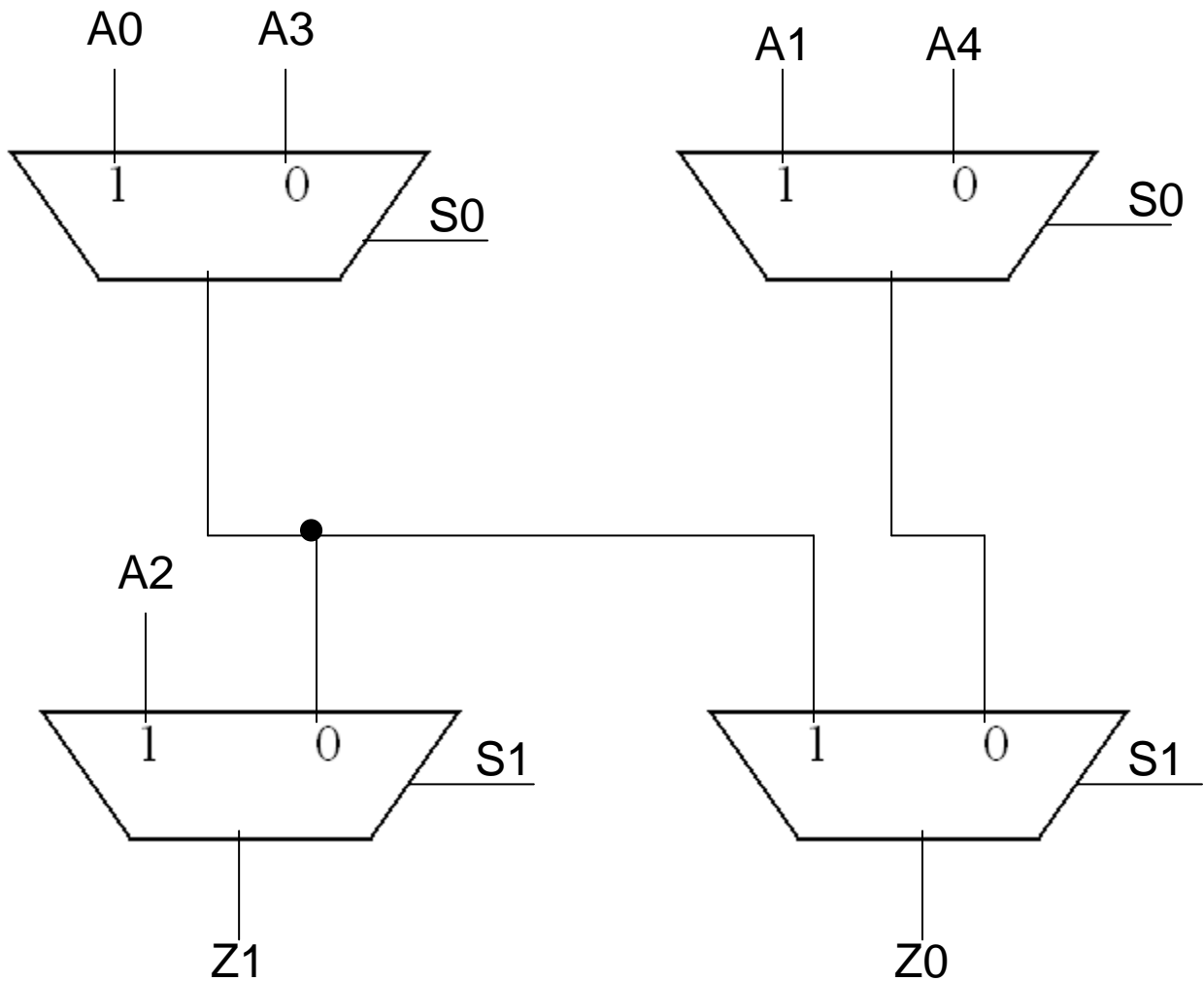
The figure below shows a combinational logic circuit. Complete the truth table corresponding to this circuit.



Inputs			Output
A	B	C	Z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Problem 5 (6 points)

The figure below shows a combinational logic circuit using for 2-to-1 multiplexers. If $S_0 = 0$ and $S_1 = 0$, what are the values of Z_1 and Z_0 ? Express your answer in terms of A_4 , A_3 , A_2 , A_1 , and A_0 .



$S_0 = 0, S_1 = 0$

$Z_1 =$ _____ A_3 _____

$Z_0 =$ _____ A_4 _____

Problem 6 (3 points)

I. Fill out the following truth table.

A	B	NOT(NOT(A) OR NOT(B))
0	0	0
0	1	0
1	0	0
1	1	1

II. What single logic gate has the same truth table?

Answer: An AND gate

Problem 7 (8 points)

This problem is similar to the in class example of the finite state machine for a cash-register. In particular, note:

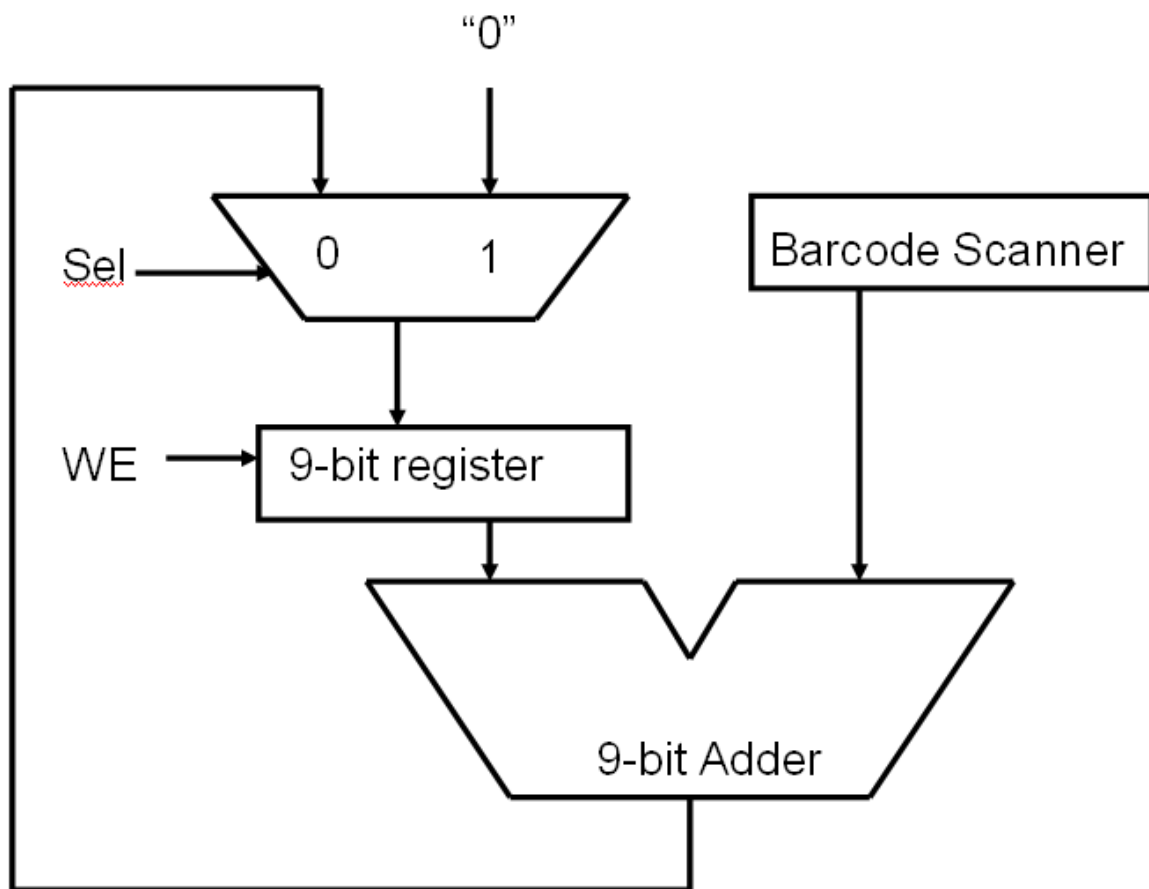
Inputs: Customer (0 – No Customer, 1 – Customer at cash-register)

Scan (0 – Nothing being scanned, 1 – Scanning Item)

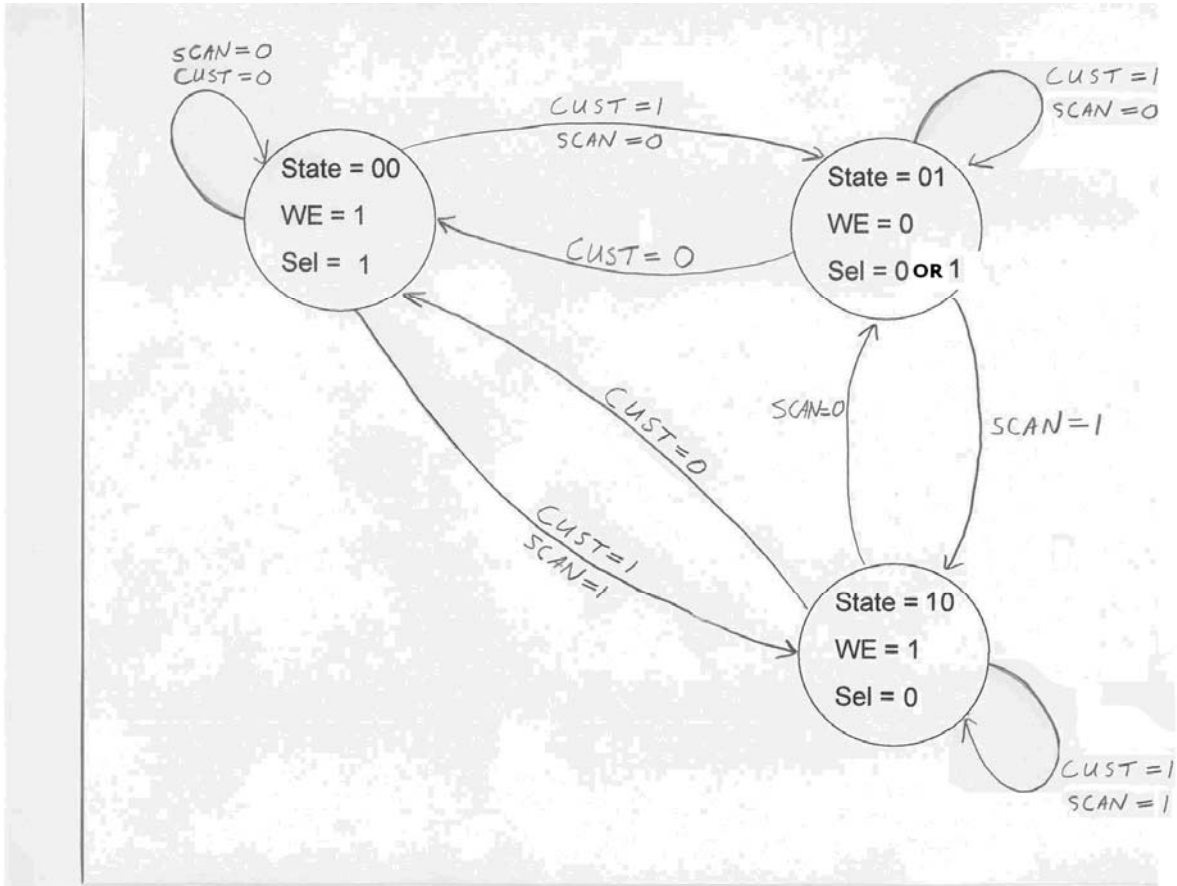
Outputs: WE-Write Enable (0 – Not enabled, 1 – Enabled)

Sel (0 – Multiplexer Input 0 Selected, 1 – Multiplexer Input 1 Selected)

For this problem, we will only need three states: 1) No customer and no scanning, 2) A customer has arrived and is not scanning, and 3) The customer is present and scanning an item. We will also assume that a customer can arrive and begin to scan an item RIGHT AWAY. Each time an item is scanned, if the Sel and WE are selected, we will compute the sum of the previous value stored in the register to the value that is scanned. For this problem, we also assume that everything is represented in DOLLARS ONLY for computing the total bill.



- I. Draw the finite state machine diagram for the cash-register. You should only need the three states provided.



- II. What happens if a customer's current bill is \$455 and they scan an item worth \$10?

It will add the total like normal.

- III. What happens if a customer's current bill is \$455 and they scan an item worth \$100?

It will cause an overflow/you will get free groceries.

Problem 8 (8 points)

Circle the correct answer for the following questions:

I. Which is NOT one of the 6 phases of the Instruction Cycle?

- a. Fetch Operands
- b. Memory Data Register
- c. Store Result
- d. Evaluate Address

Answer: b

II. Which of the following is NOT an example of a Combinational Logic Circuit?

- a. Decoder
- b. D-Latch
- c. Mux (multiplexer)
- d. Full adder

Answer: b

III. The minimum number of transistors required to implement a CMOS 3 input NAND gate is

- a. 3
- b. 8
- c. 6
- d. 4

Answer: c

IV. If a memory memory uses 8-bit words and 8-bit addressing, how many D-Latches are needed for the memory?

- a. 4096
- b. 1024
- c. 2048
- d. 8192

Answer: c