

## Using Operate Instructions

With only ADD, AND, NOT...

| How do we subtract? | How do we OR? |
| :--- | :--- |
| Subtract: R3 $=$ R1 - R2 | OR: R3 $=$ R1 OR R2 |
| Take 2'sC of R2, then add | Use DeMorgan's Law |
| (1) R2 $=N O T(R 2)$ | (1) R1 $=\operatorname{NOT}(R 1)$ |
| (2) R2 $=R 2+1$ | (2) R2 $=\operatorname{NOT(R2)}$ |
| (3) R3 $=R 1+R 2$ | (3) R3 $=$ R1 AND R2 |
|  | (4) R3 $=\operatorname{NOT(R3)}$ |

How do we copy from one register to another?
Register-to-register copy: R3 = R2 R3 = R2 + 0 (Add-immediate)
How do we initialize a register to zero?
Initialize to zero: R1 = 0 R1 = R1 AND 0 (And-immediate)

Review: Instruction Set Architecture
ISA = All of the programmer-visible components and operations of the computer

- memory organization
- address space -- how may locations can be addressed?
$>$ addressibility -- how many bits per location?
- register set
$>$ how many? what size? how are they used?
- instruction set
$>$ opcodes
> data types
> addressing modes
ISA provides all information needed for someone that wants to write a program in machine language
(or translate from a high-level language to machine language).

Review: Data Movement Instructions
Load -- read data from memory to register

- LD: PC-relative mode
- LDR: base+offset mode
- LDI: indirect mode NEW

Store -- write data from register to memory - ST: PC-relative mode

- STR: base+offset mode
- STI: indirect mode NEW

Load effective address -- compute address, save in register

- LEA: PC-relative mode
- does not access memory




## 

Control Instructions
Used to alter the sequence of instructions
(by changing the Program Counter)
Conditional Branch

- branch is taken if a specified condition is true > signed offset is added to PC to yield new PC
- else, the branch is not taken
$>P C$ is not changed, points to the next sequential instruction
Unconditional Branch (or Jump)
- always changes the PC

TRAP

- changes PC to the address of an OS "service routine" - routine will return control to the next instruction (after TRAP)

JMP (Register)
Jump is an unconditional branch -- always taken.

- Target address is the contents of a register.
- Allows any target address.

JMP 1 | 15 | 1 | 0 | 0 | 0 | 0 | 0 | Base | 0 | 0 | 0 | 0 | 0 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |



|  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| TRAP |  |  |  |  |
| $\text { TRAP } \begin{array}{\|llll\|llll\|l\|l} \hline 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & \text { trapvect } \\ \hline \end{array}$ |  |  |  |  |
|  |  |  |  |  |
| Calls a service routine, identified by 8-bit "trap vec |  |  |  |  |
| vector |  | routine |  |  |
|  | x23 | input a character from the keyboard |  |  |
|  | x21 | output a character to the monitor |  |  |
|  | x25 | halt the program |  |  |

## When routine is done,

PC is set to the instruction following TRAP. (We'll talk about how this works later.)




